WIDEBAND SOFTWARE DEFINED RADIO (SDR) DESIGN USING FIELD PROGRAMMABLE GATE ARRAYS (FPGAs)

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3rd Integrated CNS Conference and Workshop

Wideband Software Defined Radio (SDR) Design using FPGAs

Agenda

- *Why Wideband SDR for CNS?*
- *The Wideband SDR System*
  - *RXR / TXR Subsystem Architecture*
  - *A/D and D/A Subsystems*
  - *A/D Interfacing to the RXR*
  - *D/A Interfacing to the TXR*
  - *FPGAs for DSP Processing Power*
  - *DSP Design to FPGA Implementation*
- *Advances in the Near Future*
- *An Example Wideband SDR System: ECM Test Bed*
- *Applying Wideband SDR Technology for CNS*
- *Closing*

Wideband Software Defined Radio (SDR) Design using FPGAs

Why Wideband Software Defined Radio (SDR) for CNS?

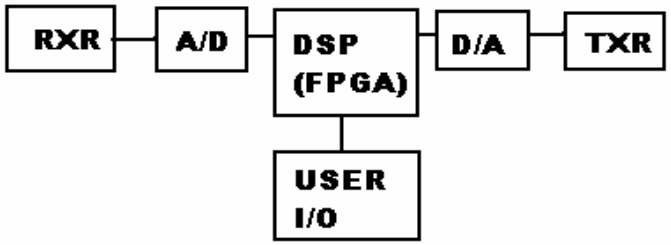
- *Re-Configurable CNS functions in Software at Baseband*
- *Great for Research, Development & Test:*
  - *Algorithms can be developed and refined in Software prior to release, no hardware changes required.*
- *Great for Operational Systems:*
  - *Improvements can be implemented on existing systems*
  - *Example: FPGAs can be configured as easily as updating the database in a GPS/Avionics receiver!*
- *Wideband SDR:*
  - *Processes more spectrum and can therefore perform more CNS functions*
  - *Utilizes advances in FPGAs, A/Ds & D/As to achieve performance*
  - *More functions accomplished at the expense of requiring more FPGA resources for DSP*

Why Wideband Software Defined Radio (SDR) for CNS?

- The High Performance of FPGAs and their advantages
  - Very High Throughput devices available (capable of >1.0 GByte/sec)
  - Parallel processing capability is highly useful for implementing very fast real-time functions such as Navigation with low latency requirements
  - Algorithm Development and Programming supports Object Oriented Design and Fixed Intellectual Property (IP) Cores. Entire CNS functions could be developed, tested and certified in terms of IP Cores

Wideband Software Defined Radio (SDR) Design using FPGAs

The Wideband SDR System

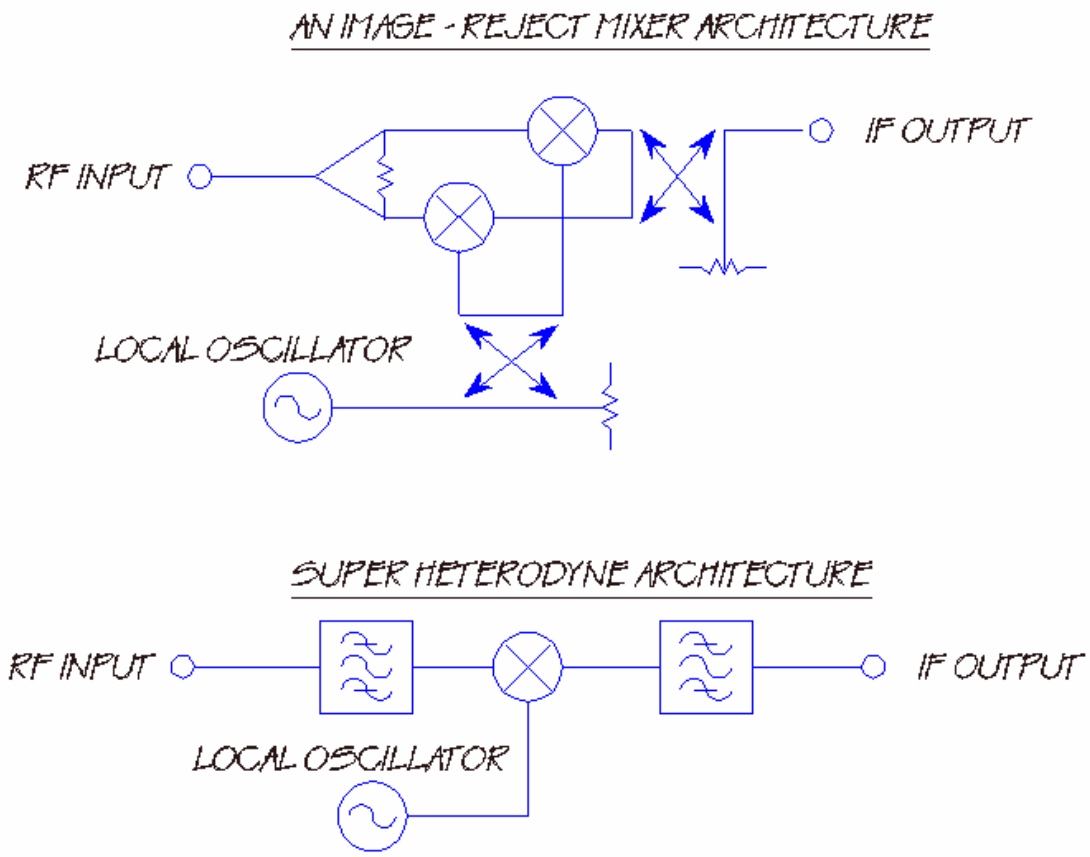


- *RXR/TXR Subsystem (Fixed H/W)*
- *A/D Subsystem (Fixed H/W)*
- *DSP (FPGAs) Subsystem (Re-Configurable S/W)*
- *D/A Subsystem (Fixed H/W)*
- *User I/O Subsystem (Re-Configurable S/W with some Fixed H/W)*

The Wideband SDR System

- *Typical System Level Performance Considerations:*
  - *Signal Types for Processing (Comm., Radar, etc.)*
  - *Linear and Non-Linear Operation*
  - *Frequency Range (Tunable and Instantaneous BW)*
  - *RXR Dynamic Range*
  - *RXR Sensitivity*
  - *TXR Output Power*
  - *TXR Spurious Emission*
  - *A/D to FPGA to D/A Throughput*
  - *User I/O to/from FPGA*
  - *Required DSP Processing capabilities (Channelization, Latency, etc.)*
  - *Other such as power, environment, TSO/MIL-STDs, etc*

RXR/TXR Subsystem Architecture

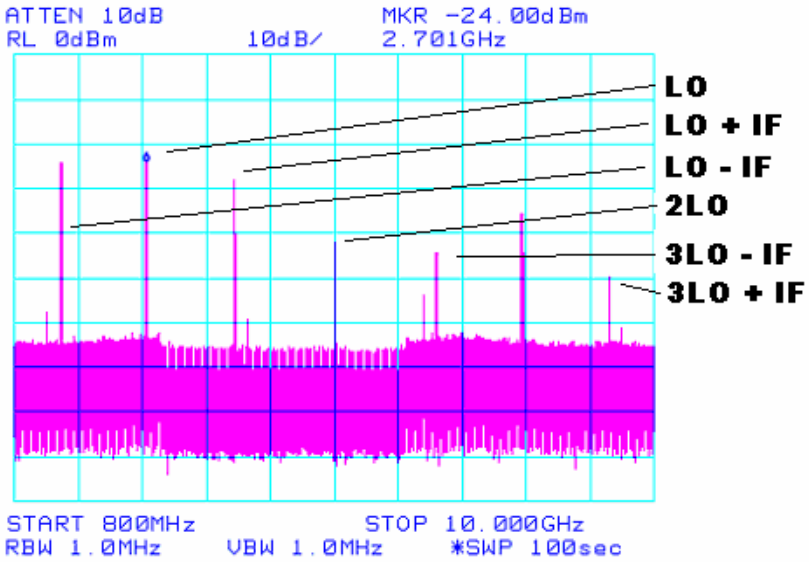


RXR/TXR Subsystem Architecture

- *RXR/TXR Architecture selection based on the SDR system requirements and required RXR/TXR precision. Defined by the existing NAS System it must interface with such as VHF/UHF Comm./Nav, VDL, ADS-B, etc. (Analog or Digital Comm., Radar, Nav, other)*
- *Image-Reject Mixer Architecture*
  - *Typ. 20 – 30 dB Image Rejection. Rejection decreases with increasing IF bandwidth*
- *Super Heterodyne Architecture*
  - *> 60 dB Spurious and Image Rejection capable at the expense of dedicated filtering (more hardware impacts size, weight, etc.)*
- *Other Architectures Exist: Direct Conversion, etc.*

RXR/TXR Subsystem Architecture

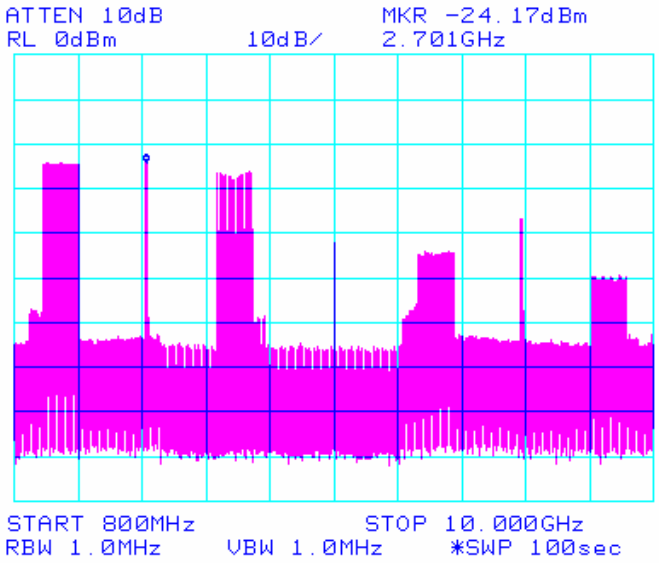
Typical Narrowband Mix: 1.27 GHz LO x 1.25 GHz w/ 10 MHz BW



- *Mixing scheme requires careful selection to avoid unwanted mixer Images. Wideband RXR/TXR design yields wideband images*

RXR/TXR Subsystem Architecture

Wideband Mix: 1.27 GHz LO x 1.25 GHz w/ 500 MHz BW



- *As the desired mixer image increases in bandwidth, so do the undesired mixer images.*

RXR/TXR Subsystem Architecture

- *Many choices are available for wideband COTS components (triple balanced mixers, broadband couplers, etc.) including high dynamic range components.*

- *Wideband RXR pays a performance penalty in terms of a higher noise floor (kTB):*
  - *Noise Floor of a RXR w/ 25 MHz BW = -100 dBm*
  - *Noise Floor of a RXR w/ 500 MHz BW = -87 dBm*

RXR/TXR Subsystem Architecture

- **Other RXR/TXR Performance Characteristics:**
  - Gain
  - Noise Figure
  - Third Order Intercept
  - Second Order Intercept
  - 1 dB Compression Point
  - Minimum Discernable Signal (MDS) Level
  - Linear and Non-Linear Dynamic Range
  - Intermodulation Product Output Level
  - S/N Ratio
  - Phase Noise
  - Phase Coherency
  - Anti-Aliasing and Anti-Imaging Filters
  - Automatic Gain Control (AGC)
  - Tunable Operating Range

A/D and D/A Subsystems

- A/Ds (and D/As) have a sampling frequency and a resolution

- Nyquist criteria determines the required sampling and locates Nyquist sampling zones at integer multiples of N starting from DC. We can use the following formula to calculate the Nth Nyquist zone:

$$NZ = N \times 0.5 \times f_S$$

- NZ is the upper limit of the Nth Nyquist Zone(1st, 2nd, 3rd, etc.)
- N is an integer greater than or equal to 1
- fs is the sampling frequency
- Example: An A/D with a sampling frequency of 1.5 GHz:
  - 1st NZ from DC to 750 MHz (Non-Inverted Spectrum)
  - 2nd NZ from 750 MHz to 1.5 GHz (Inverted Spectrum)

A/D and D/A Subsystems

Design Notes

- *The spectrum of odd numbered Nyquist zones (1st, 3rd, etc.) is a correct representation of the spectrum of the sampled bandwidth. Even numbered Nyquist zones (2nd, 4th, etc.) represent an inverted spectrum of the sampled bandwidth*
- *Practical operation of A/Ds and D/As can only work the first several Nyquist zones. Beyond the first few Nyquist zones, the A/D performance decreases and it is unusable for sampling at higher frequencies.*
- *Nyquist criteria means that whatever the full bandwidth is we wish to process, we must use a sample frequency at twice the highest bandwidth, regardless of the Nyquist zone in which it is sampled.*
- *Undersampling, IF Sampling and similar terms refer to sampling a signal other than in the 1st Nyquist zone. Oversampling refers to sampling a signal within the first Nyquist zone.*
- *A/D and D/A clock jitter can have a greater impact on system performance when IF Sampling versus oversampling.*

A/D and D/A Subsystems

- A/Ds and D/As have a sampling speed and resolution. The sampling speed determines the width of the Nyquist Zones.

High FPGA Throughput + Faster Sample Rates = More SDR BW

- The conversion of an Analog signal to a Digital representation (and vice-versa) introduces errors. Some typical A/D subsystem performance considerations:
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise and Distortion (SINAD)
  - Noise Power Ratio (NPR)
  - Quantization Error
  - A/D Clock Jitter / Phase Noise

A/D and D/A Subsystems

- A/Ds are currently higher in speed than the fastest D/As, but D/A performance is also increasing
- D/As have similar performance considerations when converting from a Digital signal to an Analog signal. Some performance considerations include:
  - Sin(X)/X Roll-Off
  - SFDR
  - Transmit S/N Ratio
  - D/A Clock Jitter / Phase Noise
  - D/A Clock to D/A Output Frequency
  - DSP processing throughput to D/A
  - Built-In D/A Interpolation and/or Filtering functions

A/D Interfacing to the RXR

- *Interfacing between the A/D and RXR Subsystems:*
  - *For many SDR systems, the SFDR of the A/D can be matched to the Noise Floor of the RXR for sensitivity*
  - *Matching usually requires the RXR Subsystem Gain is adjusted to meet a fixed performance A/D (COTS)*
  - *Account for Linear and Non-Linear Operation if required*
  - *Account for AGC operation*

A/D Interfacing to the RXR

$$V_{PK} = \sqrt{P_{RMS} \times Z_O \times 2}$$

- ***A useful matching formula for Interfacing the A/D to the RXR and the D/A to the TXR:***
  - $Prms$ ***is the RMS Power in (Watts)***
  - Zo ***is the Transmission Line Impedance (Ohms)***
  - Vpk ***is the Peak Voltage of a perfect sinusoid***

D/A Interfacing to the TXR

- *Interfacing between the D/A and TXR Subsystems:*
  - *Similar process to the A/D & RXR Interface*
  - *Determine Linear and Non-Linear Operation if required*
  - *Match the D/A maximum output to maximum required TXR input at baseband*
  - *Matching usually requires the TXR Subsystem Gain is adjusted to a fixed performance D/A (COTS)*

FPGAs for DSP Processing Power

- *FPGAs have made significant performance increases in the last few years. Currently available in 8 Million and 10 Million system gates (Xilinx Virtex 2 8000 and Virtex 2 10000) and clock speeds reaching hundreds of MHz*
  - *The architecture of these devices has been tailored for DSP processing*

- *Wideband SDR requires FPGAs because of the tremendous throughput:*
  - *An 8-bit A/D with a sampling frequency of 1.5 GHz is transmitting 1.5 GByte/sec!*
  - *FPGAs are well suited to Real-Time "pipelined" DSP functions (FFTs, etc).*
  - *Can be used in hybrid configuration with Programmable DSPs, but the processing load for SDR generally demands that FPGAs are required at the front end of the SDR*

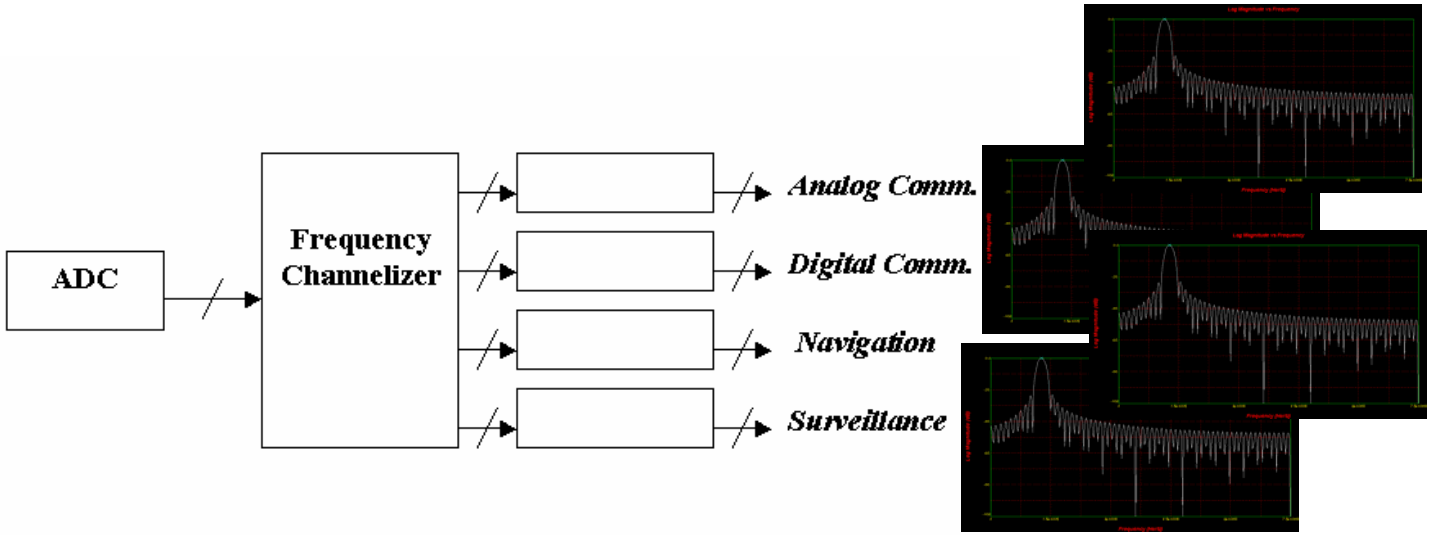
DSP Design to FPGA Implementation

- *Wideband SDR: A DSP block (subsystem) level design is used to determine basic CNS functions, including control and interface to the User I/O subsystem.*

- *The DSP block design is modeled and a rough estimate of SDR functions is performed to determine the amount of FPGA resources required to implement the design.*
  - *Actual resources required depends on many implementation specifics (IP Core, Custom S/W, etc.) and any post Place & Route Optimization*

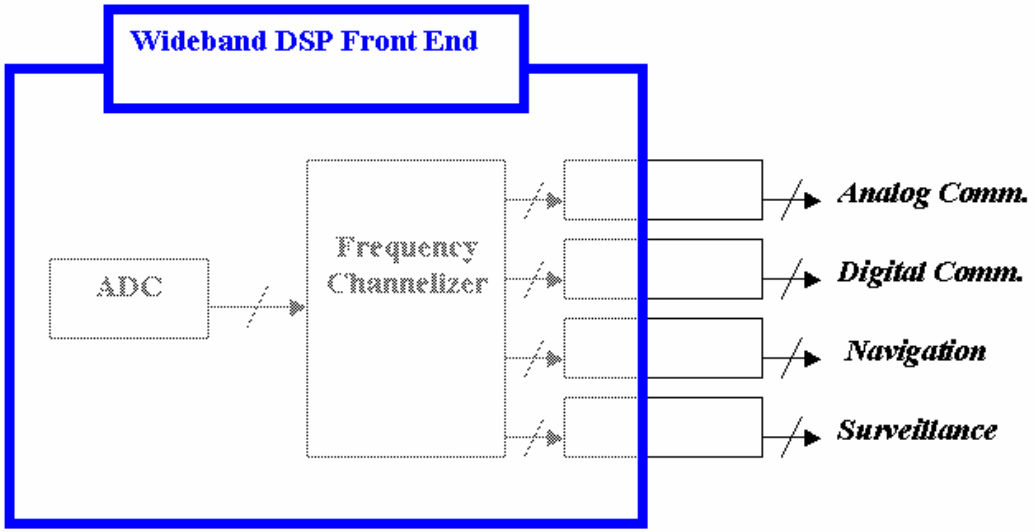
DSP Design to FPGA Implementation

- *Wideband SDR required to perform more than a single function requires frequency channelization to "break-up" the spectrum for specific processing task…*
  - *FPGAs provide independent parallel implementation and real-time performance*



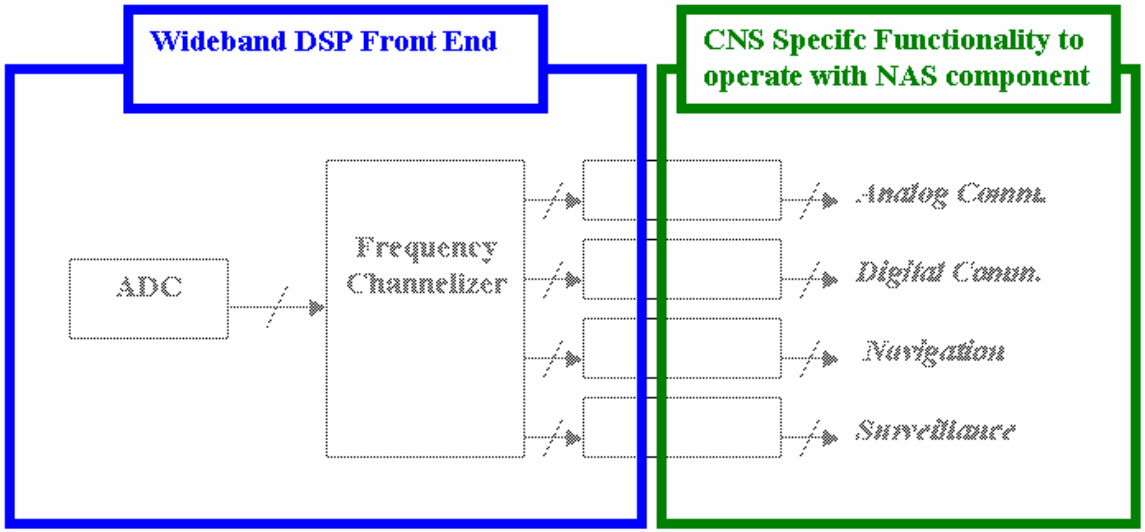
DSP Design to FPGA Implementation

- *Wideband SDR requires the Channelization of the sampled spectrum into narrowbands for processing…*
  - *A Wideband DSP Front End Implemented in FPGAs Polyphase filters and Cascade Integrator Comb (CIC or a.k.a Hogenauer filter) perform high decimation while filtering and are very useful for Wideband SDR*



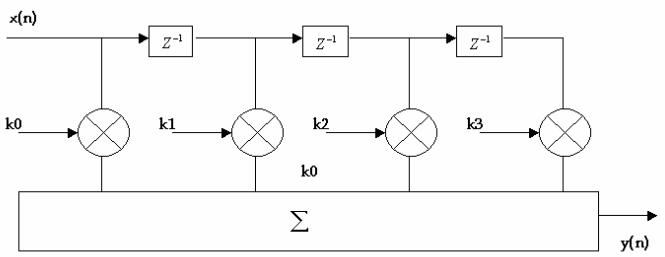
DSP Design to FPGA Implementation

- *Wideband SDR requires the Channelization of the sampled spectrum into narrowbands for processing…*
  - *After Channelization and decimation, CNS Specific functions can be implemented. Overall functionality and performance must meet system level / NAS component requirements*



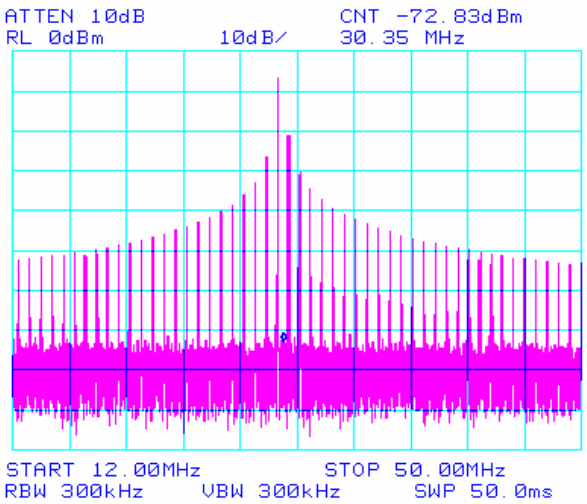
DSP Design to FPGA Implementation

- *FPGAs are today's high performance DSP engines and can implement many DSP components for SDR…*
  - *FFTs*
  - *Digital Down/Up Conversion*
  - *Digital Filters / Decimators*
  - *Coordinate Rotation Digital Computer (CORDIC) Algorithm*
  - *Hilbert Transforms*
  - *Phase Locked Loops / Costas Loops*
  - *Phase Quadrature Conversions*
  - *Many more…*

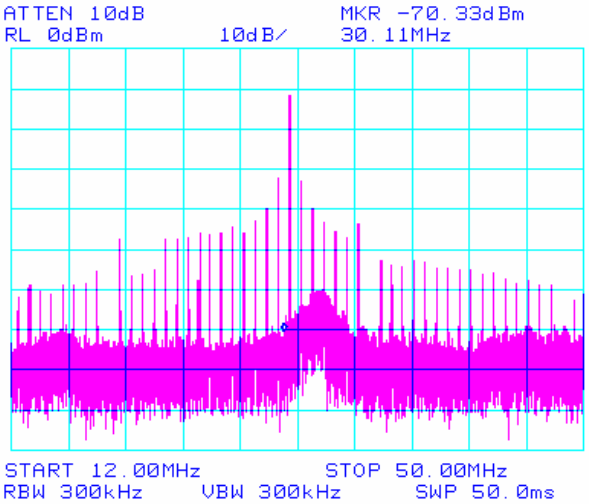


DSP Design to FPGA Implementation

- **FPGAs can deliver real-time performance, here an RF pulse is sampled at baseband, stored to memory and re-transmitted…**
  - **FPGAs can generate complex CNS waveforms in real-time**



Incident RF Pulse



RF Pulse Echo

Advances in the Near Future

- *FPGAs are continuing to increase in performance and capabilities. Increasing performance and Multi-GByte throughput will push the demand for SDR to process more of the spectrum*

- *FPGA Verification and Implementation typically has been technically challenging, but this is changing due to the next generation of FPGA Implementation tools such as CoreFire by Annapolis Micro Systems. As FPGA Technology proliferates, the availability and performance of these tools is expected to increase*

- *A/D and D/A performance is also increasing (higher sampling speeds, higher resolution, lower distortion). The availability of higher performance, COTS hardware will also push the demand for SDR to process more of the spectrum*

Wideband Software Defined Radio (SDR) Design using FPGAs

An Example Wideband SDR System: ECM Test Bed

- *BOOZ | ALLEN | HAMILTON CONTRACTED BY THE US ARMY INTELLIGENCE AND INFORMATION WARFARE DIRECTORATE (I2WD) TO DESIGN AND BUILD AN ADVANCED TECHNOLOGY, HIGH PERFORMANCE SYSTEM TO ACT AS A TESTBED TO EXPLORE ELECTRONIC COUNTERMEASURES (ECM) FROM 20 MHz TO 40 GHz*

- *HIGH-PERFORMANCE, FLEXIBLE, DIGITAL-BASED TESTBED DEVELOPMENT FOR THE ANALYSIS, TESTING, EVALUATION AND GENERATION OF A VARIETY OF COMMUNICATIONS AND RADAR SIGNALS OF INTEREST*

- *TESTBED ARCHITECTURE BASED UPON:*
  - *SOFTWARE FULLY RE-CONFIGURABLE FIELD PROGRAMMABLE GATE ARRAYS (FPGAs)*
  - *HARDWARE RE-CONFIGURABLE RF/MICROWAVE RECEIVER/TRANSMITTER (RXR/TXR)*

An Example Wideband SDR System: ECM Test Bed

- THE OBJECTIVE WAS TO DEVELOP A FULLY RE-CONFIGURABLE (FLEXIBLE), HIGH BW ELECTRONIC COUNTERMEASURES (ECM) TOOL CAPABLE OF RESEARCHING, ANALYZING, SIMULATING AND PRODUCING COMPLEX COMMUNICATIONS AND RADAR WAVEFORMS

- THE RESULTING SYSTEM IS A STATE-OF-THE-ART WIDEBAND, SOFTWARE DEFINED RADIO. THIS TECHNOLOGY IS USEFUL AS A RESEARCH AND ANALYSIS TOOL FOR THE EVALUATION OF SIGNALS FOR LABORATORY-BASED DEVELOPMENT WITH A DESIGN APPROACH EXPANDABLE TO FIELD USE OR PROTOTYPE AS WELL
  - HIGH BANDWIDTH/HIGH THROUGHPUT CAPABILITIES (500+ MHz INSTANTANEOUS RXR BANDWIDTH)
  - PROGRAMMABLE DSP/FPGA AND ARCHITECTURE

Applying Wideband SDR Technology for CNS

- *Small to Large variants of this fully re-programmable wideband system are available for a wide range of applications*
  - *Custom systems can be provided to cover over the entire 20 MHz - 40 GHz or for specific frequency bands*
  - *Generic or fully customized FPGA algorithms can be developed and provided with the system. BAH can provide full FPGA algorithm development and support.*
- *Support Technology Research and Development*
- *Support Lab/Field Performance Evaluation of Technology*
- *Flexible architecture means the User can reprogram the system to adapt and meet a wide range of current and future needs*
- *As a high performance, flexible and fully re-programmable tool, this class of system supports the User in becoming a solutions provider to manage the development and application of SDR technology*

Applying Wideband SDR Technology for CNS

- *System designs can be tailored to meet specific requirements and applications for CNS:*
  - *Research, Analysis, Development and Test Tool*
  - *Stand alone system to study and develop proof-of-concept technology*
  - *Bolt-on interface to existing systems to enhance signal processing performance (Low cost, high performance system upgrade or life cycle extension).*
  - *Stand Off, Real-Time, Operational Test and Evaluation tool for characterization and analysis, or signal generation for developmental or existing operational systems.*
  - *System Re-programmability delivers full flexibility and capability. System FPGAs can be fully re-programmed by the User to analyze, characterize and test the performance many types of waveforms and systems without having to redesign or change hardware.*

Closing

- *This concludes our system level discussion of "Wideband SDR Design using FPGAs".*

"Thank You"

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